REMARKS

Claims 1-19 are presented for further examination.

Notice of References Cited

Applicant again requests that the Examiner address the following issue regarding the Notice of References Cited. This issue was raised in applicant's prior responses, but was not addressed by the Examiner.

Listed reference N in the Notice of References Cited that accompanied the Office action of July 24, 2009 is EP555886 (Kuwata). The country associated with this reference appears to be incorrectly listed on the Notice of References Cited. In particular, it appears the country should be listed as Europe (not Japan).

Also, U.S. Patent No. 6,365,925 (Hase), which is cited in the Office action of November 29, 2010 against some of the claims, does not appear to be listed on the Notice of References Cited.

Applicant respectfully requests that a corrected or supplemental Notice of References Cited be provided correctly listing EP555886 (Kuwata) and US 6,365,925 (Hase).

Rejections under 35 U.S.C. §§102-103

Claims 10, 12 and 19

Claims 10, 12 and 19 were rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 4,807,011 (Nonaka). Reconsideration is requested.

A finding of anticipation requires that a single prior art reference disclose *each and every* limitation of the claim. MPEP §2131. As explained below, that is not the case here.

Independent claim 10 recites a buffer layer "on" a channel region in a first conductivity type first semiconductor layer. An example is illustrated in FIG. 1, which shows buffer layer 3 on the channel regions under the p+ regions 4a, 4b. (*See* Specification at page 10, lines 17-18).

In contrast, Nonaka discloses a semiconductor IC circuit in which the high-resistivity region 22 (which the Office alleges corresponds to the claimed "buffer layer") is arranged below the channel region 18a (*see* FIG. 3, reproduced below).

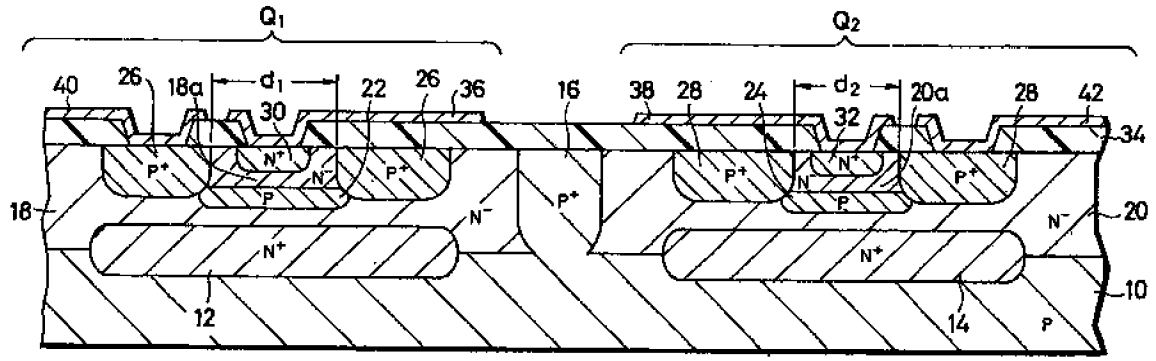

FIG. 3

Therefore, Nonaka fails to disclose a buffer layer "on the channel region" as recited in claim 10.

The Office argues (at pages 2 and 19 of the action), however, that the area under the gate region 26 and above the buried layer 12 also forms part of the "channel region," and that, therefore, the buffer layer (i.e., high-resistivity region 22) is "on" the channel region. As explained below, that is incorrect. In particular, the area under the gate region 26 and above the buried layer 12 does not form part of the "channel region."

First, Nonaka itself specifically identifies only the region 18a (and the corresponding region 20a) as serving as a "channel region." *See, e.g.*, col. 5, lines 40-41; 48-50. There is nothing in Nonaka to indicate that the region under the gate region 26 and above the buried layer 12 is either called a channel region or serves as a channel region. Furthermore, Nonaka expressly states that the lateral dimension of channel region 18a is indicated by d_1 (col. 4, lines 49-61; FIG. 3). The dimension does not extend to areas that are under the gate region 26 and above the buried layer 12.

In addition, a person of ordinary skill in the art would have understood that the channel region of Nonaka's vertical SIT refers to a region that (i) is present in the path through which carriers flow from the source region into the drain region (*see* col. 3, lines 54-55), and (ii) in which the amount of carriers present in the relevant region is controlled by the voltage applied to the gate region (*see* col. 3, lines 51-53). As expressed by Nonaka (col. 3, lines 50-55):

> As described above, in a SIT, the potential in the channel region, i.e. the space charge region, is controlled by a bias voltage which is applied to the gate region, whereby the amount of the carriers which flow from the source region into the drain region is controlled.

Thus, the carriers flowing from the source region to the drain region in the vertical SIT shown in FIG. 3 of Nonaka flow in a direction vertical to the principal surface of the semiconductor substrate (col. 4, lines 41-44). This means that the opposing buried layer 12 immediately under source region 30 is the drain region (or, alternatively, region 30 is a drain region and region 12 is a source region) (*see* col. 7, lines 62-65). The region under p^+ gate region 26 is <u>not</u> located at a region between the source region and the drain region and, therefore, does <u>not</u> satisfy the first criteria defining the channel region as set forth above. Furthermore, since p^+ gate region 26 can be in contact with buried region 12 (*see* col. 5, lines 66-68), the region under p^+ gate region 26, even if not present, will not affect the operation as the SIT of device Q1. Therefore, the region under p^+ gate region 26 does not satisfy the second criteria defining the channel region as set forth above. Thus, the channel region in device Q1 shown in FIG. 3 of Nonaka includes regions

18a and 20a, but does not include the areas under the gate region 26 and above the buried layer 12.

At least for this reason, the rejections of claims 10, 12 and 19 should be withdrawn.

Furthermore, another distinction indicates that the claims recite very different subject matter from that disclosed by Nonaka. In particular, Nonaka's buffer layer 22 extends vertically to the direction of the carrier flow from the source region to the drain region in channel region 18a. Thus, in contrast to the buffer layer of the present application, Nonaka's buffer layer 22 does not function to control the carrier concentration in the channel region.

Claims 1, 2, 4 and 18

Claims 1, 2, 4 and 18 were rejected under 35 U.S.C. §103(a) as obvious from U.S. Patent No. 5,161,235 (Shur) in view of U.S. Patent No. 6,365,925 (Hase). Reconsideration is requested.

Independent claim 1 recites that a second conductivity type doped region extends into the first conductivity type first semiconductor layer to a top surface of the buffer layer, but does not extend through the buffer layer. An example is illustrated in FIG. 1 of the present application which shows that the second conductivity type doped regions 4a, 4b extend into the first conductivity type semiconductor layer 1 to the top surface of the buffer layer 3. The regions 4a, 4b do not, however, extend through the buffer layer 3. The claimed feature(s) can provide various advantages such as those discussed in the specification at page 11, line 13 – page 12, line 17 and at page 14, line 5 – page 15, line 9.

Shur discloses a FET designed to increase barrier height and reduce turn-on threshold (title; abstract; col. 3, lines 38-64). The Office acknowledges that Shur fails to disclose a second conductivity type doped region extending into the first conductivity type first semiconductor layer. The Office argues, however, that Hase discloses this feature and that it would have been obvious to modify Shur in view of Hase to obtain the claimed subject matter.

Applicant disagrees for at least the following reasons. Even if there were some reason to modify Shur in view of Hase, at most that might have led a person of ordinary skill to extend Shur's gate 6 (which the Office alleges corresponds to the claimed "second conductivity type doped region") into the quantum well region 4 (which the Office alleges corresponds to the

claimed "first conductivity type first semiconductor layer"). For ease of reference, FIG. 5(L) of Shur is reproduced below.

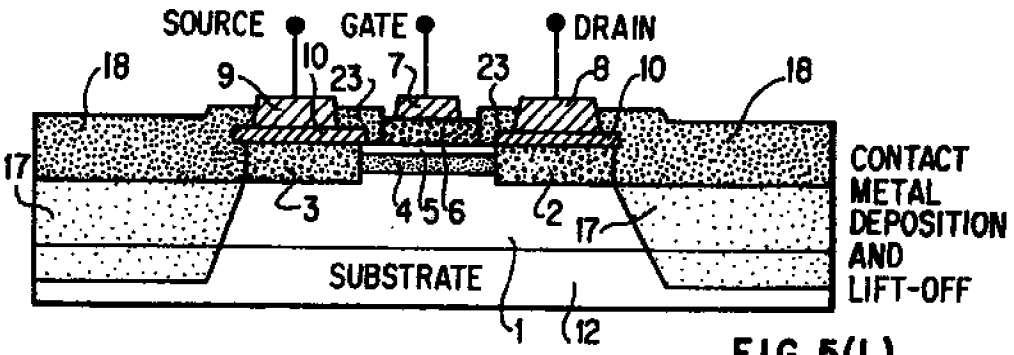

FIG. 5(L)

Assuming there were some reason to extend Shur's gate 6 into the quantum well region 4 (which applicant does not concede), that would not have resulted in, or rendered obvious, the subject matter of claim 1.

The Office argues (at page 19 of the action) that a portion of the gate electrode 6 in FIG. 5L of Shur could be slightly extended so as to result in the gate electrode 6 extending into semiconductor layers 2 and 3 without extending through buffer layer 5. That is clearly incorrect. A person of ordinary skill would readily recognize and understand that, in a plan view, the n-type regions 2 and 3 are not located at an overlapping region between the gate electrode 6 and barrier layer 5. Therefore, even if the gate electrode 6 slightly extended into the barrier layer 5, it would absolutely not extend into n-type regions 2 and 3. The entire premise of the Office action in arguing that one could extend the gate electrode 6 into the semiconductor layers 2, 3 makes no sense whatsoever.

Furthermore, as previously explained, if Shur's gate 6 were extended into the quantum well region 4, then the gate 6 would extend through the barrier layer 5 (which the Office alleges corresponds to the claimed "buffer layer"). Thus, the combination of Shur and Hase would not have rendered obvious the claimed subject matter including "a second conductivity type doped region extending into the first conductivity type first semiconductor layer to a top surface of the buffer layer, but not extending through the buffer layer."

At least for the foregoing reasons, the rejections of claim 1, as well as claims 2, 4 and 18, should be withdrawn.

Claims 3 and 5-9

- Claims 3, 5-7 and 9 were rejected under 35 U.S.C. §103(a) as obvious from Shur in view of Hase and further in view of U.S. Patent Publication No. 2003/0075719 (Sriram).
- Claim 8 was rejected under 35 U.S.C. §103(a) as obvious from Shur in view of Hase and Sriram and further in view of U.S. Patent Publication No. 2005/0139859 (Kumar I).

Claims 3 and 5-9 depend, directly or indirectly, from claim 1. None of the other references, including Sriram and Kumar I, disclose the features missing from Nonaka discussed above, and there would have been no reason to modify Nonaka in view of any of these references to obtain the claimed subject matter. Therefore, the rejections of claims 3 and 5-9 should be withdrawn.

Claims 11 and 13-17

- Claims 11 and 15-16 were rejected under 35 U.S.C. §103(a) as obvious from Nonaka in view of U.S. Patent No. 6,841,812 (Zhao).
- Claims 13 and 14 were rejected under 35 U.S.C. §103(a) as obvious from Nonaka in view of U.S. Patent Publication No. 2002/0139992 (Kumar II).
- Claim 17 was rejected under 35 U.S.C. §103(a) as obvious from Nonaka in view of Zhao and Sriram.

Claims 11 and 13-17 depend, directly or indirectly, from claim 10. None of the other references, including Sriram, Kumar II and Zhao, disclose the features missing from the combination of Shur and Hase discussed above, and there would have been no reason to modify

Shur and Hase in view of any of these references to obtain the claimed subject matter. Therefore, the rejections of claims 11 and 13-17 should be withdrawn.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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